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Application No. 09/722,404
Response to Office Action dated May 28, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of the Claims:

Claim 1 (Currently Amended): A semiconductor storage device storing regular data and having a security function for preventing unauthorized use of the regular data, comprising:

a first store including a first storing area for fixedly storing a first portion of the regular data and a dummy data storing area for fixedly storing dummy data in place of a second portion of the regular data, the second portion of the regular data being necessary for use of the regular data;

a second store including a second storing area which has have a storage capacity equal to at least a storage capacity of the dummy data storing area of the first store storing means and fixedly stores the second portion of the regular data to be originally stored in the dummy data storing area; and

a read control circuit which compares an input address with a dummy address corresponding to the dummy data of an address space of the dummy data storing area[[, to enable]] and which enables reading of the first portion of the regular data from the first store when the input address and the dummy address do are not correspond identical, and disables to disable the reading of the first portion of the regular data and enables enable the reading of the second portion of the regular data from the second store when the input address and the dummy address correspond are identical.

Claim 2 (Currently Amended): A semiconductor storage device according to claim 1, wherein the first store includes a masked ROM, and the second store includes a an nonvolatile semiconductor memory which is a writable/readable memory.

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Claim 3 (Currently Amended):   A semiconductor storage device according to claim 2, wherein the nonvolatile semiconductor memory has a storage capacity larger than the ~~a~~ storage capacity of the second regular data storing area, and further includes a dummy address storing area, ~~for storing the dummy address~~ other than the second storing area, for storing the dummy address ~~regular data storing area~~, and the dummy address supplied ~~to be applied~~ to the read control circuit ~~means~~ is read from the dummy address storing area.

Claim 4 (Currently Amended):   A semiconductor storage device according to claim 3, wherein the ~~semiconductor~~ nonvolatile semiconductor memory is constructed such that ~~the~~ data is written with a first write voltage in the second regular data storing area and the dummy address storing area, and ~~the~~ data is written with a second write voltage lower than the first write voltage in other areas.

Claim 5 (Currently Amended):   A semiconductor storage device according to claim 1, wherein the read control circuit includes a comparator ~~comparitor~~ for comparing the input address and the dummy address with each other to output a first signal or a second signal, an enabling/disabling circuit for enabling the first store in response to the first signal and disabling the first store in response to the second signal, and a read address output circuit for outputting a read address for the second portion of the regular data ~~being~~ stored in the second store in response to the second signal.

Claim 6 (Currently Amended):   A semiconductor storage device according to claim 2, wherein the ~~semiconductor~~ nonvolatile semiconductor memory and the read control circuit are ~~is~~ formed within the same single memory chip.

Claim 7 (Currently Amended):   A memory device ~~cartridge~~ storing an application program and having a security function for preventing unauthorized use of the application program, comprising:

a first store including a first program storing area for fixedly storing a first portion of the application program and a dummy data storing area for fixedly storing dummy data in place of a

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second portion of the application program, the second portion of the application program being necessary for use of the application;

a second store including a second program storing area which has ~~have~~ a storage capacity equal to at least a storage capacity of the dummy data storing area of the first store and fixedly stores the ~~a~~ second portion of the application program ~~to be originally stored in the dummy data storing area~~; and

a read control circuit which compares an input address with a ~~the~~ dummy address corresponding to ~~data of~~ an address space of the dummy data storing area, and which enables ~~to enable~~ reading of the first portion of the application program from the first store when the input address and the dummy address do ~~are~~ not correspond ~~identical,~~ and disables ~~to disable~~ the reading of the first portion of the application program and enables ~~enable~~ the reading of the second portion of the application program from the second store when the input address and the dummy address correspond ~~are identical~~.

Claim 8 (Currently Amended): An electronic device for storing an application program and having a security function for preventing unauthorized use of the application program, comprising:

a first store including a first program storing area for fixedly storing a first portion of the application program and a dummy data storing area for fixedly storing dummy data in place of a second portion of the application program, the second portion of the application program being necessary for use of the application program;

a second store including a second program storing area which has ~~have~~ a storage capacity equal to at least a storage capacity of the dummy data storing area of the first store and fixedly stores the ~~a~~ second portion of the application program ~~to be originally stored in the dummy data storing area~~; and

a read control circuit which compares an input address with a ~~the~~ dummy address corresponding to ~~data of~~ an address space of the dummy data storing area and which enables, ~~to enable~~ reading of the first portion of the application program from the first store when the input address and the dummy address do ~~are~~ not correspond ~~identical,~~ and disables ~~to disable~~ the reading of the first portion of the application program and enables ~~enable~~ the reading of the

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second ~~portion of the~~ application program from the second store when the input address and the dummy address corrected ~~are identical~~.

Claim 9 (Currently Amended):   A memory device ~~cartridge~~ for a game machine storing a game program and having a security function for preventing unauthorized use of the game program, comprising:

a first store including a first program storing area for fixedly storing a first portion of the game program and a dummy data storing area for fixedly storing dummy data in place of a second portion of the game program, the second portion of the game portion being necessary for use of the game program;

a second store including a second program storing area which has ~~have~~ a storage capacity equal to at least a storage capacity of the dummy data storing area of the first storing means and fixedly stores the ~~a~~ second portion of the game program ~~to be originally stored in the dummy data storing area~~; and

a read control circuit which compares an input address with a ~~the~~ dummy address corresponding to ~~data of~~ an address space of the dummy data storing area and which enables ~~to enable~~ reading of the first portion of the game program from the first store when the input address and the dummy address do ~~are~~ not correspond ~~identical~~, and disables ~~to disable~~ the reading of the first portion of the game program and enables ~~enable~~ the reading of the second portion of the game program from the second store when the input address and the dummy address correspond ~~are identical~~.

Claim 10 (Currently Amended):   A memory device ~~cartridge for a game machine~~ according to claim 9, wherein the first store includes a masked ROM, and the second store includes a ~~an~~ nonvolatile semiconductor memory which is a writable/readable memory.

Claim 11 (Currently Amended):   A memory device ~~cartridge for a game machine~~ according to claim 10, wherein the nonvolatile semiconductor memory has a storage capacity larger than the ~~a~~ storage capacity of the second ~~regular data~~ storing area, and further includes a dummy address storing area, ~~for storing the dummy address~~ other than the second regular data

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storing area, <u>for storing the dummy address,</u> and the dummy address <u>supplied</u> ~~to be applied~~ to the read control circuit is read from the dummy address storing area.

Claim 12 (Currently Amended): A memory <u>device</u> ~~cartridge for a game machine~~ according to claim 11, wherein the nonvolatile semiconductor <u>memory</u> is constructed such that the data is written in the second game program storing area and the dummy address storing area with a first write voltage and ~~the~~ data is written with a second write voltage lower than the first write voltage into other areas, <u>and</u> in the storing area into which the data is written with the second write voltage, ~~and~~

backup data representing a development of the game obtained by executing the ~~first~~ game program ~~and/or the second game program~~ by a processor of <u>the</u> ~~a~~ game machine is written.

Claim 13 (Currently Amended): A memory <u>device</u> ~~cartridge for a game machine~~ according to claim 9, wherein the read control circuit includes a <u>comparator</u> ~~comparitor~~ for comparing the input address and the dummy address with each other to output a first signal or a second signal, an enabling/disabling circuit for enabling the first store in response to the first signal and disabling the first store in response to the second signal, and a read address output circuit for outputting a read address for the second <u>portion of the game program</u> ~~regular data being~~ stored in the second store in response to the second signal.

Claim 14 (Currently Amended): A method for preventing unauthorized use of regular data stored in a storage device comprising ~~the steps of~~:
storing in a first storage area <u>a</u> first <u>portion of the</u> regular data and storing dummy data in a dummy data area of said first storage area <u>in place of a second portion of the regular data, the second portion of the regular data being necessary for use of the regular data;</u>
storing in a second storage area having a storage capacity equal to at least a storage capacity of the dummy data storing area of the first storage area <u>the</u> second <u>portion of the</u> regular data ~~to be originally stored in the dummy data storing area~~; and
comparing an input address with <u>a</u> ~~the~~ dummy <u>address corresponding to</u> ~~data of~~ an address space of the dummy data storing area <u>and enabling,</u> ~~to enable~~ reading of the first <u>portion</u>

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of the regular data from the first storage area when the input address and the dummy address do are not correspond identical, and disabling to disable the reading of the first portion of the regular data and enabling enable the reading of the second portion of the regular data from the second storage area when the input address and the dummy address correspond are identical.

Claim 15 (Currently Amended):   A method according to claim 14, wherein the first storage area resides in a masked ROM, and the second storage area resides in a an nonvolatile semiconductor memory which is a writable/readable memory.

Claim 16 (Currently Amended):   A method according to claim 15, wherein the nonvolatile semiconductor memory has a storage capacity larger than a storage capacity of the second regular data storing area, and the method further includes including the step of storing a dummy address in a dummy address storing area, and reading the dummy address from the dummy address storing area.

Claim 17 (Currently Amended):   A method according to claim 15, further including the step of writing to the semiconductor nonvolatile semiconductor memory with a first write voltage in certain areas thereof, and writing with a second write voltage lower than the first write voltage in other areas thereof.

Claim 18 (Currently Amended):   A method according to claim 15, further including the steps of comparing the input address and the dummy address with each other to output a first signal or a second signal, and enabling the first storage area in response to the first signal and disabling the first storage area store in response to the second signal, and outputting a read address for the second portion of the regular data being stored in the second storage area in response to the second signal.

Claim 19 (New):   A storage device adapted to provide security for a video game program stored therein, comprising:

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a video game program memory for storing a first part of the video game program, and for storing dummy data at one or more predetermined locations thereof;

a memory separate from the video game program memory for storing a second part of the video game program, the second part of the video game program being a part that is predetermined to be necessary for use of the video game program so that copying of the first part of the video game program and the dummy data from the video game memory will not provide an operable video game program;

memory control circuitry for controlling the video game program memory and the separate memory, wherein the memory control circuitry compares an address input thereto from a video game program executing system with an address for the separate memory, enables output from the video game program memory if the input address and the address for the separate memory do not correspond, and disables output from the video game program memory and enables output from the separate memory if the input address and the address for the separate memory correspond.

Claim 20 (New):   The storage device according to claim 19, wherein the memory control circuitry comprises an output disabling circuit for disabling the output of the video game program memory if the input address and the address for the separate memory correspond.

Claim 21 (New):   The storage device according to claim 20, wherein the output disabling circuit comprises a logic circuit.

Claim 22 (New):   The storage device according to claim 19, wherein the video game program memory and the separate memory are embodied on different chips.

Claim 23 (New):   The storage device according to claim 19, wherein the video game program memory is disabled in response to a chip select signal if the input address and the address for the separate memory correspond.

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Claim 24 (New):   The storage device according to claim 19, wherein the separate memory comprises a first portion in which data is written using a first writing voltage and a second portion in which data is written using a second, different writing voltage.

Claim 25 (New):   The storage device according to claim 24, wherein the first voltage is higher than the second voltage and the second part of the video game program is stored in the first portion of the separate memory.

Claim 26 (New):   The storage device according to claim 25, wherein the first voltage is a voltage different than a writing voltage of video game program executing system so that the video game program executing system cannot write to the first portion of the separate memory.

Claim 27 (New):   The method according to claim 25, wherein the second voltage is a voltage equal to a writing voltage of the video game program executing system and the video game program executing system selectively writes game back-up data to the second portion of the separate memory using the second voltage.

Claim 28 (New):   A method for providing security for a video game program stored in a storage device, the method comprising:

storing a first part of the video game program in a video game program memory of the storage device;

storing dummy data at one or more predetermined locations of the video game program memory;

storing a second part of the video game program in a memory of the storage device separate from the video game program memory, the second part of the video game program being predetermined to be a part necessary for use of the video game program so that copying of the first part of the video game program and the dummy data from the video game program memory will not provide an operable video game program, wherein

an address input to the storage device from a video game program executing system is compared with an address for the separate memory;

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access to the video game program memory is enabled if the input address and the address for the separate memory do not correspond; and

access to the video game program memory is disabled and access to the separate memory is enabled if the input address and the address for the separate memory correspond.

Claim 29 (New):   The method according to claim 28, wherein the separate memory comprises a first portion in which data is written using a first writing voltage and a second portion in which data is written using a second, different writing voltage

Claim 30 (New):   The method according to claim 29, wherein the first voltage is higher than the second voltage and the second part of the video game program is stored in the first portion of the separate memory.

Claim 31 (New):   The method according to claim 30, wherein the first voltage is a voltage different than a writing voltage of the video game program executing system so that the video game program executing system cannot write to the first portion of the separate memory.

Claim 32 (New):   The method according to claim 30, wherein the second voltage is a voltage equal to a writing voltage of the video game program executing system and the video game program executing system selectively writes game back-up data to the second portion of the separate memory using the second voltage.